

## UNIVERSITAS GADJAH MADA

Faculty of Mathematics and Natural Sciences

Department of Computer Science and Electronics Sekip Utara Bulaksumur Yogyakarta 55281 Telp: +62 274 546194 Email: <u>dep-ike.mipa@ugm.acid</u> Website: <u>http://dcse.fmipa.ugm.acid</u>

## **Bachelor in Electronics and Instrumentation**

Telp Email : +62 274 546194 : kaprodi-s1-elins.mipa@ugm.ac.id Website : http://dcse.ugm.ac.id/

## **MODULE HANDBOOK**

Module name	Computer Organization and Architecture					
Module level	Undergraduate					
Code	MII-1601					
Courses (if	Computer Organization and Architecture					
applicable)						
Semester	Summer (Even)					
Contact person	Abdul Ro'uf					
Lecturer	Abdul Ro'uf					
	Bambang N. Prastowo					
Language	Bahasa Indonesia					
Relation to	1. Undergraduate degree program, compulsory, 2th semester.					
curriculum	2. International undergraduate program, compulsory, 2th semester.					
Type of teaching,	1. Undergraduate degree program: lectures, < 60 students,					
contact hours	2. International undergraduate program: lectures, < 30 students.					
Workload	1. Lectures: $2 \times 50 = 100$ minutes (1 hours 10 menit) per week.					
	2. Exercises and Assignments: $2 \times 50 = 100$ minutes per week.					
	3. Private study: $2 \times 50 = 100$ minutes per week.					
Credit points	2 credit points (sks).					
Requirements	A student must have attended at least 75% of the lectures to sit in the					
according to the	exams.					
Examination						
regulations						
Recommended	-					
prerequisites						
Learning outcomes	After completing this module, a student is expected to:					
(course outcomes)	CO1 Able to explain the basic concepts of computer organization and					
and their	architecture and its development to date					
corresponding PLOs	CO2 Be able to describe and identify instruction sets and their execution,					
	as well as methods to increase execution speed.					
	CO3 Able to explain the basic principles of processor implementation,					
	the basic operations of the control unit and how to control					
	execution in pipeline and parallel.					
	CO4 Able to explain memory hierarchy, and able to calculate increase in memory performance.					
	CO5 Able to explain parallel processor architecture and its development					
	to date in multicore form.					

	PLC	) (	CO	CO	CO	CO	C05	]
			1	2	3	4		
	Program	PLO1						
	Learning	PLO2						
	Outcome	PLO3						
	(PLO)	PLO4						
		PLO5						
	1 1 4 1 4					1,	1 1	
Contents	<ol> <li>Introduction: Abstracts of computer systems and technology</li> <li>Instruction Execution of stored-program computer's</li> </ol>							
	3. Processor, d	atapath and co	ntro	l unit w	ith pipe	eline		
	4. Memory hie	•						
	5. Parallel proc							
Study and	The evaluation is done in 3 forms, namely:							
examination	· · ·	er midterm or s			,			
requirements and		s, individual as	sign	ments t	o be co	mplete	d within	a certa
forms of examination	timeframe, and							
	3. Two quizzes, held on face-to-face, once before midterm exam and							
	once after midterm exam, with a short answer form.							
Madia ang lawad	measuring the rank.			derstan	ding re	lated to	the targ	et and o
Media employed Assessments and	LCD, blackboa	ard, and websit	les.					
Evaluation	Туре	Percenta	ge	CO1	CO2	CO 3	CO4	C05
	Quiz	5 %		$\checkmark$		$\checkmark$		
	Individual Ta	sk 25 %					$\checkmark$	
		SK					1	1
	Group Task	0						
	Group Task Midterm Exa	0						
	<b>_</b>	0					√	√
	Midterm Exa	0 m 40 %			N	√	√	√
Reading List	Midterm Exan Final Exam <b>Total</b> [1] David A. F Organizati Interface, [2] David A. F	0       m     40 %       30 %     100%       Patterson and J       Ion and Design       1st Edition, Mo	RIS orga ohn	L. Hen SC-V E n Kauf L. Hen	nessy, 2 dition: ' mann. nessy, 2	2017, C The Ha 2016, C	computer rdware S	c Softwar

Designing for Performance, 11th Edition, Pearson.	