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MODULE HANDBOOK

Module name	**Embedded System Experiment**
Module level, if applicable	Undergraduate
Code, if applicable	MII 2324
Courses, if applicable	Embedded System Experiment
Semester(s) in which the module is taught	Odd
Person responsible for the module	Tri Wahyu Supardi, S.Si., M.Cs
Lecturer(s)	Tri Wahyu Supardi, S.Si., M.Cs
Language	English and Indonesia
Relation to curriculum	1.Undergraduate degree program, optional, 3rd semester. 2.International undergraduate program, optional, 3rd semester.
Teaching methods	Case-Based Learning
Workload (incl. contact hours, self-study hours)	1. Lectures: 1 x 50 = 150 minutes per week. 2. Exercises and Assignments: 1 x 50 = 100 minutes per week. 3. Private study: 1 x 50 = 50 minutes per week.
Credit points	1
Requirements according to the examination regulations	Minimum attendance at lectures is 75% (according to UGM regulation). Final score is evaluated based on practice experiments (35 %), experiment report (35%), and final exam (30%).
Required and recommended prerequisites for joining the module	
Learning outcomes and their corresponding PLOs	After completing this module, a student is expected to: (CO-1): Able to understand and do the stages of FPGA-based hardware development (CO-2): Able to use CAD tool for FPGA development (CO-3): Able to model hardware of various descriptions (CO-4): Able to carry out functional verification and measure hardware performance on FPGA platforms (CO-5): Able to analyze the needs of embedded system design and its implementation

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<tr><th colspan="2">PLO</th><th>CO1</th><th>CO2</th><th>CO3</th><th>CO4</th><th>CO5</th></tr>
<tr><td rowspan="5">Program Learning Outcome (PLO)</td><td>PLO1</td><td>√</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>PLO2</td><td>√</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>PLO3</td><td></td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>PLO4</td><td></td><td></td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>PLO5</td><td></td><td></td><td></td><td></td><td></td></tr>
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<tr><td>Content</td><td>1. Introduction of FPGA development
2. Introduction of FPGA Development Software
3. Circuit Design on FPGA Development Software
4. Simulation and analysis of FPGA Circuit Design
5. Implementation and analysis of FPGA Circuit Design</td></tr>
<tr><td>Study and examination requirements and examination forms</td><td>The evaluation is done in 3 forms, namely:
1. Practice
2. Report
3. Final Exam
Assessment is done using benchmark assessment, with the aim of measuring the level of student understanding related to the target and class rank.</td></tr>
<tr><td>Media employed</td><td>e-learning Platform, LCD, glass board, and websites.</td></tr>
<tr><td>Assessments and evaluation</td><td>
<table>
<tr><th>Type</th><th>Percentage</th><th>CO1</th><th>CO2</th><th>CO3</th><th>CO4</th><th>CO5</th></tr>
<tr><td>Practice</td><td>35</td><td>√</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>Experiment report</td><td>35</td><td>√</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
<tr><td>Final Exam</td><td>30</td><td>√</td><td>√</td><td>√</td><td>√</td><td>√</td></tr>
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<tr><td>Total</td><td>100</td><td></td><td></td><td></td><td></td><td></td></tr>
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<tr><td>Reading list</td><td>

Gajski, Daniel D, Abdi., Samar, Gerstlauer., Andreas., Schirner, Gunar., 2010.
Embedded System Design Modeling, Synthesis and Verification, University of California, Springer
RECRLab (Reconfigurable Computing Research Laboratory), VHDL Coding for FPGAs, Electrical and Computer Engineering Department, Oakland University
Digilent, 2013, Nexys3™ Board Reference Manual, www.Digilentinc.com, 3 Maret 2014

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Revision date	**:**	